6. THE CLAIMS

It is claimed:

1. A method of determining at least one transistor fanout, the method comprising:

   a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a dynamic resistor;

   b) determining a steady state solution to the sizing model; and

   c) determining at least one transistor fanout from the steady state solution.

2. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current.

3. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logical element.

4. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a voltage.

5. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic

resistor the size of which is based at least upon a current and a voltage.

6. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logic element, a current, and a voltage.

7. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of a current.

8. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the logical effort of a logic element.

9. The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the inverse of a voltage.

10. A device containing machine-readable instructions, that when executed perform a method of determining at least one ratio of transistor sizes, the method comprising:

a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a dynamic resistor;

b) determining a steady state solution to the sizing model; and

c) determining at least one transistor fanout from the steady state solution.

11. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current.

12. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logical element.

13. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a voltage.

14. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current and a voltage.

15. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic

resistor the size of which is based at least upon the logical effort of a logic element, a current, and a voltage.

16. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of a current.

17. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the logical effort of a logic element.

18. The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the inverse of a voltage.

19. An integrated circuit created at least in part by a method of determining at least one ratio of transistor sizes, the method comprising:

a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a dynamic resistor;

b) determining a steady state solution to the sizing model; and

c) determining at least one transistor fanout from the steady state solution.

20. The integrated circuit of claim 19, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current.

21. The integrated circuit of claim 19, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logical element.

22. The integrated circuit of claim 19, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a voltage.